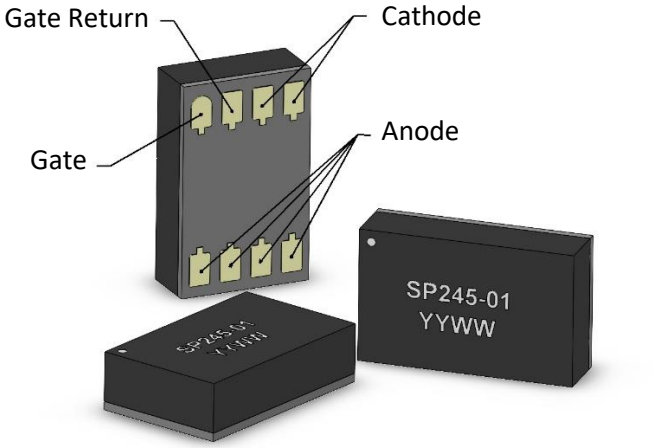
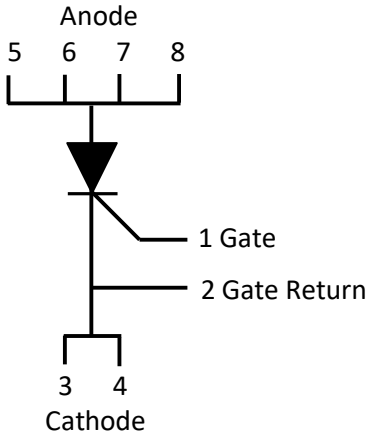
SP245-01

Solidtron™ Solid State Initiator Firing Switch, C-Pak

***NOTICE:* This product is export controlled**





Description

The **Solidtron™ SP245-01** is an advanced high-voltage current-controlled thyristor packaged in a **C-Pak** custom SMT package.

Like all Solidtron™ products, the internal semiconductor employs high cell density and an advanced termination design to achieve high peak current capability, low conduction loss, low off-state leakage, negligible turn-on delay jitter, and most importantly, extremely high turn-on dI/dt capability. It is ideally suited for a wide variety of capacitor discharge applications requiring precise timing and rapid energy transfer capability.

The C-Pak is a custom surface mount package in which the semiconductor is attached to a metalized ceramic substrate using 90Pb10Sn solder, wire bonded using 0.010” aluminum wire bonds, and then, encapsulated using Hysol FP4653 epoxy. The C-Pak is specifically designed to comply with IPC 2221 Section 6.3 Electrical Clearance (any elevation).

The SP245-01 is intended to replace triggered spark gaps of similar voltage and current ratings.

Features

- 1500V Repetitive Off-State Voltage
- VGK = 0V = OFF-STATE
- 100 kA/µs dI/dt capability
- Low Turn-on Delay Time
- Low Conduction Loss
- 3.5kA Repetitive Surge Current

Applications

- LEEFI detonators
- Electronic Safe and Arm Devices
- Ignition Safety Devices
- Firing Modules
- Capacitor Discharge Units

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Table 1 Maximum Ratings	Symbol	Value	Units
Repetitive Peak Off-State Voltage	V_{DRM}	1500	V
Repetitive Peak Reverse Voltage	V_{RRM}	-10	V
Off-State Rate of Change of Voltage Immunity (V_D=1500V)	dv/dt	1000	V/µSec
Peak Non-Repetitive Surge Current (1/2 Sinusoid Pulse Duration =/<300nSec)	I_{TSM}	4000	A
Peak Repetitive Surge Current (1/2 Sinusoid Pulse Duration =/<300nSec)	I_{TRM}	3500	A
Rate of Change of Current	dI/dt	100	kA/µSec
Critical Capacitor Discharge Event Integral (Underdamped LCR Circuit)	$I^2t_{CRITICAL}$	TBD	A^2sec
Repetitive Capacitor Discharge Event Integral (Underdamped LCR Circuit)	$I^2t_{REPETITIVE}$	2	A^2sec
Continuous Gate-Cathode Reverse Voltage	V_{GKS}	-9	V
Forward Peak Gate Current (10□Sec Duration)	I_{GM}	10	A
Required Off-State Gate-Cathode Voltage	V_{GDM}	0	V
Operating Junction Temperature Range	T_J	-55 to +125	°C
Maximum Soldering Installation Temperature *(See Moisture Sensitivity Caution)*		220	°C
Storage Temperature Range *(See Moisture Sensitivity & Solderability Cautions)*		-55 to +150	°C

Table 2 Electrical Characteristics				Measurements			
Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Anode to Cathode Breakdown Voltage	V_{BR}	V_{GK}= 0V, I_D=100µA, T_C ≤ 125°C		1500			V
Anode-Cathode Forward Off-State Current ***See Figure 2.***	I_{DRM}	V_{GK}= 0V, V_D=1500V	T_C=-55°C			60	nA
			T_C=25°C		10	100	nA
			T_C=85°C		190	1000	nA
			T_C=125°C		5	10	µA
Reverse Bias Gate-Cathode Breakdown Voltage	V_{GRRM}	I_{GM}=150µA, T_C≤ 125°C		9	10		V
Nine Volt Reverse Bias Gate-Cathode Leakage Current ***See Figure 1.***	I_{GM}	V_{GK}= -9V	T_C=25°C		28		µA
			T_C=85°C		57		µA
			T_C=125°C		80		µA
Two Volt Reverse Bias Gate-Cathode Leakage Current ***See Figure 1.***	I_{GM}	V_{GK}= -2V	T_C=25°C		0.8	2	µA
			T_C=85°C		1.9	4	µA
			T_C=125°C		2.4	6	µA
Gate Trigger Voltage	V_{GT}	V_D= 12V, I_D=1mA	T_C=25°C	450	500		mV
			T_C=85°C	250	350		mV
			T_C=125°C	200	250		mV
Gate Trigger Current	I_{GT}	V_D= 12V, I_D=1mA, T_C ≤ 125°C				100	µA
Turn-on Delay Time	$t_{d(ON)}$	0.15µF Capacitor Discharge, T_C=25°C, I_{GT}= 500mA, V_{DD}=1200V, L_S=15nH, R_S=0.010Ω=CVR			30	60	nSec
Rate of Change of Current	dI/dt				65		kA/µsec
Capacitor Discharge Event Integral	I^2t				1.38		A^2sec
Peak Anode Current	I_{DM}				3.2		kA

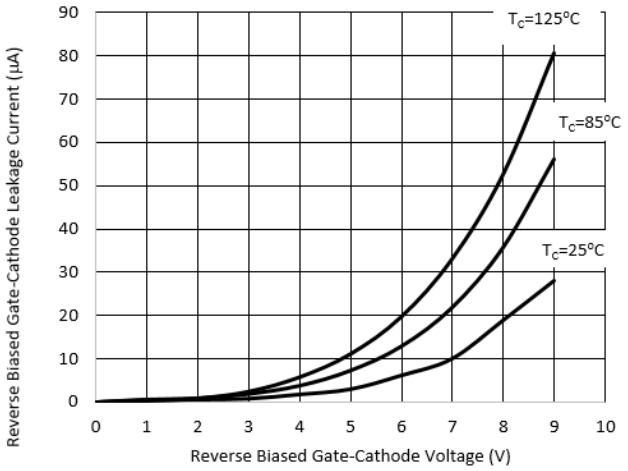


Figure 1 Typical Reverse Biased Gate-Cathode Leakage Characteristic

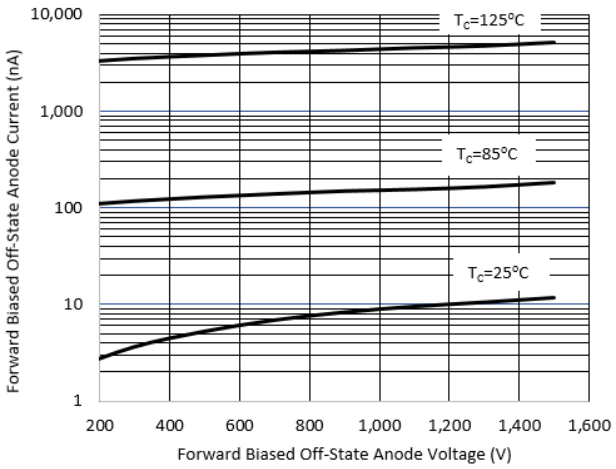


Figure 2 Typical Forward Biased Off-State Anode-Cathode Leakage Characteristic

Usage

The Gate Return pad provides a dedicated connection directly to the cathode of the semiconductor die. This connection consists of a single 0.010" aluminum wire bond. Using the Gate Return pad as an independent gate driver return path reduces V=L*dI/dt stress on the gate driver components. With C-Pak Solidtron™ devices, the Gate Return may, alternatively, be used as an additonal Cathode pad; however, its internal connection possesses only 40% of the I^2t capability of each of the other Cathode pads. Using it in this fashion must be qualified by the customer for their specific application.

ESD Sensitivity

The **SP245-01** has been tested IAW **MIL-STD-883 ESD-HBM (Human Body Model) to +/-2000V (Class 1C).**

The **SP245-01** has been tested IAW **ANSI/ESDA/JEDEC/JS-002-2014 for ESD-CDM (Charged Device Model) to +/-1500V (Class C5).**

Moisture Sensitivity

The **SP245-01** have been tested IAW **IPC/JEDEC J-STD-020** and are classified as **MSL Level 5A.**

In accordance with **IPC/JEDEC J-STD-033**, **C-Pak** products are dry-baked and immediately packed in a Moisture Barrier Bag (MBB) containing desiccant and a Humidity Indicator Card (HIC). When the Moisture Barrier Bag is opened or compromised refer to **IPC/JEDEC J-STD-033** for proper HIC interpretation, floor life and storage procedures.

Although **IPC/JEDEC J-STD-033** prescribes specific dry-baking temperatures and times, caution is advised as additional baking of C-Pak SMD packages may cause oxidation and/or intermetallic growth of the terminations which may result in solderability problems during board installation. The temperature and time for baking this SMD package should, therefore, be limited with solderability considerations in mind. If available, it is recommended C-Paks be baked in a nitrogen or vacuum oven to limit exposure to oxygen during the baking process.

Solderability

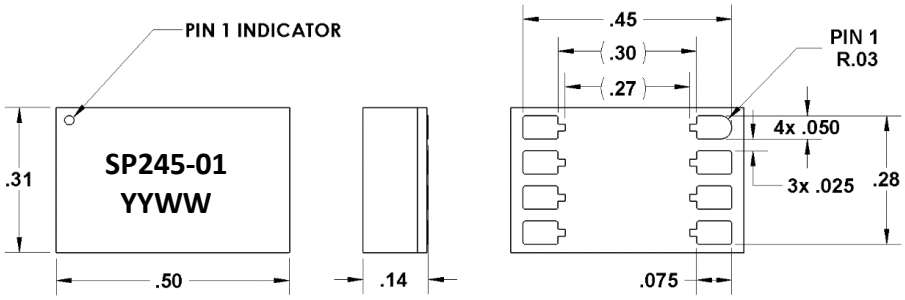
Although the component pads of the **SP245-01** appear to be gold plated, exposure to high process temperatures within the manufacturing process have accelerated the diffusion of the underlying nickel into and through the thin exterior gold surface, therefore, rendering the pads **subject to oxidation growth** if exposed to circumstances which

Solidtron™ SP245-01

Solderability (Continued)

promote nickel oxidation. Such circumstances should be avoided; otherwise, solderability of the **SP245-01** will be compromised.

Markings and Dimensions



DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE NOTED:
TWO PLACE DECIMAL +/- 0.010”
THREE PLACE DECIMAL +/- 0.005”

PART NUMBER
SP = SOLIDTRON™ PRODUCT
245 = CHIP TYPE
-01 = PACKAGE TYPE

DATE CODE
YY = LAST 2 DIGITS OF CALENDAR YEAR
WW = WORK WEEK

About Excelitas Technologies

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